REMARKS

The present application contains claims 1-3, 5, 6, 8, 9, 12, 13, 18-22, 23 and 25-27. Claim 13 has been amended. Claims 4, 11, 14-17, 21 and 24 have been withdrawn as being directed to non-elected subject matter.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23 and 25-27 have been rejected under 35 U.S.C. §102(b) as anticipated by Bruccoleri et al. ('488 Patent). This rejection is respectfully traversed.

The Examiner states that, regarding claims 1, 2, 18, 12 and 22, Figure 3 of Patent '488 shows a method for reducing distortion of a signal to an input of an input/output device having parasitic capacitance comprising the steps of:

detecting a change of the input voltage (high or low) at the input I+;

introducing a current when INV2 has high level output with a positive edge of the input signal to charge the parasitic capacitance Cin to compensate the current of the input signal charging said parasitic capacitance.

The Examiner notes that when the input signal voltage is below the threshold voltage of circuit input, the parasitic capacitance Cin formed by the gate-source/drain of the transistor(s) of INV1 is charged and when a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of INV1 becomes low and the output of INV2 becomes high and thus a current is introduced to the parasitic capacitor Cin to compensate for current of the input

signal that charges Cin. The Examiner further notes that the parasitic capacitance Cin is across the input and the ground.

It is submitted that the teachings of Patent '488 are not applicable to the subject matter of claims 1, 2, 18, 12 and 22.

Patent '488 teaches a latch specifically designed for use in a comparator. Making reference to Figures 2 and 3, the input and reference voltages are respectively I+ and I-, which signals are applied simultaneously to both the inputs and outputs of the inverters INV1 and INV2. More specifically, the signal I+ is applied to both the input of INV1 and the output of INV2. Similarly signal I- is applied to the input of IV2 and the output of INV1. The manner in which the circuits of Figures 2 and 3 operate is such that electronic switches S1 and S2 are controlled by signal Vck of timing pulse generator CK. Electronic switches S3 and S4 are controlled by the timing signal $\overline{Vck}$.

During a first phase, switches S1 and S2 are closed and switches S3 and S4 are open. This enables input capacitances Cin, at the inputs of INV1 and INV2, to charge to the respective levels I+ and I-. It should be noted that since switches S3 and S4 are open at this time, INV1 and INV2 do not provide any output.

During phase 2, switches S1 and S2 are opened and switches S3 and S4 are closed. The charge across each Cin at INV1 and INV2 **remains constant**. At this time, INV1 and INV2 are energized, causing the positive feedback between these

two inverters to be active. Thus, the output values U+ and U- appearing at the outputs of buffers BF1 and BF2 appear as two voltages Vout+ and Vout- which differ from one another by an amount of "even up to several hundreds of times greater than the differential input voltage due to the regenerative action of the positive feedback" (see column 3, lines 40-48 of Patent '488). It should be noted at this time that "the latch is insensitive to possible variations in the input voltages" (see column 3, lines 43 and 44). It should be noted that the only action that occurs is that these signals are amplified so that if a signal is positive it is rendered more positive and if it is negative it is rendered more negative. This operation is directly the opposite of the present invention in which, when a direction of change in voltage of an input signal is detected, a current is introduced to the parasitic capacitance to **compensate** for changes of the current of the input signal charging the parasitic capacitance, as is recited in claim 1, for example.

It is thus clear that Patent '488 not only teaches away from the present invention but teaches a device which operates in a manner opposite from the device of the present invention.

Making reference to Figures 3 and 4 of Patent '488, the parasitic capacitances are described as respectively appearing between node A and ground and between node B and ground, which nodes are respectively connected to the plus(+) power supply and ground.

The specification of Patent '488 teaches that, the as switching frequency provided by the timing pulse generator CK increases, the offset voltage of the circuitry increases. Note that the feedback in the '488 Patent is **positive** feedback and not negative feedback. See column 3, lines 59 through 65 of Patent '488.

To compensate for the undesirable effect of frequency on the offset voltage, switches S5 and S6 are provided in the embodiment of Figure 3, causing the parasitic capacitances to be discharged to prevent initiation of a positive feedback during this sampling phase. It should be noted that the parasitic capacitances CA and CB are **not** inputs to the circuit but appear between the node A and ground and between the node B and ground.

Contrary to the Examiner's statement that (each of) the capacitances Cin is charged when the input signal voltage is below the threshold voltage of the circuit input, there is no such teaching found in the '488 Patent. To the contrary, the patent simply teaches that the voltage applied to the inputs I+ and I- cause the capacitances Cin to charge. There is no threshold level described in the '488 Patent.

Claims 2 and 18 depend from claim 1 and carry all of its limitations and hence are deemed to patentably distinguish over Patent '488 for the same reasons as set forth hereinabove with regard to claim 1.

Claim 12 recites substantially the same limitations as claim 1 but differs in that claim 12 recites compensation for "distortion" of the input signal.

Claim 22 depends from claim 12 and carries all of its limitations and hence is deemed to patentably distinguish over Patent '488 for the same reasons as set forth hereinabove with regard to claims 1 and 12.

The Examiner states that, regarding claims 3, 19, 23, 13 and 27, Figure 3 of Patent '488 shows a method of reducing distortion of a signal applied to the input of circuit having a parasitic capacitance, wherein INV1 detects a direction of change in voltage in the input signal in that INV1 has a high output level and INV2 has a low output level in response to a negative edge input signal and parasitic capacitance Cin discharges through INV2 thus preventing discharging of the parasitic capacitance into the input signal, the parasitic capacitance Cin being across the input in the ground.

Applicant submits that this interpretation of this Patent '488 is not correct. Firstly, it should be noted that the '488 Patent does not refer to Cin as a parasitic capacitance but merely as an input capacitance which, in the example of the invention in Patent '488 is an important capacitance and is required in order to permit each of the input capacitances Cin to be charged to the level of the input signal and thereafter to remove the input signal in a second phase of operation during which the electronic switches S1 and S2 are opened and the switches S3 and S4 are closed in order to power the inverters INV1 and INV2.

Claim 3 recites detecting a direction of change in voltage of the input signal and preventing discharge of the parasitic capacitance responsive to detection of a negative edge of the input signal. As was pointed out hereinabove, the cross-coupled inverters INV1 and INV2 provide positive feedback so that a positive signal is made more positive and a negative signal is made more negative which is the reverse operation from that of the present invention and specifically as recited in claim 3.

Claim 19 depends from claim 3 and carries all of its limitations and hence is deemed to patentably distinguish over Patent '488 for the same reasons as set forth hereinabove with regard to claim 3.

Claim 13 recites substantially the same limitations as claim 3 except that claim 13 recites preventing introduction of current responsive to detection of a positive edge of the input signal (note that claim 13 has been amended at line 5 to change the term "negative" to read "positive").

Claim 23 also depends from claim 13 and carries all of its limitations and hence is deemed to patentably distinguish over Patent '488 for the same reasons as set forth hereinabove with regard to claims 3 and 13.

Claim 27 recites preventing discharge of the parasitic capacitance into the input of said circuit responsive to detection of a negative edge of the input signal eliminating a need for an additional parasitic capacitance to reduce distortion.

These limitations are neither taught nor remotely suggested by the '488 Patent and it is submitted that claim 27 patentably distinguishes thereover.

The Examiner states that regarding claims 5, 6 and 25, Figure 3 of Patent '488 shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency and having the parasitic capacitance comprising a detection circuit INV1 for detecting changes in the input voltage; a correction circuit INV2 coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal, the Examiner noting that when the input signal voltage is below the threshold voltage of circuit input, the parasitic capacitance Cin forming between the gate-source/drain of the transistor(s) of INV1 is charged and when a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of INV1 becomes low and the output of INV2 becomes high and thus a current is introduced to the parasitic capacitance Cin to compensate for current of the input signal that charges Cin and that the parasitic capacitance Cin is across the input and the ground, the Examiner further stating that it is inherent that the detection circuit INV1 includes a capacitance directly connecting to one terminal of the parasitic capacitance.

It is again submitted that the teachings of Patent '488 has no bearing on the present invention since the circuits INV1 and INV2 are not detection and correction

circuits but are circuits which provide regentative positive feedback in order to significantly increase the amplitude or output level of two output signals provided in a comparator circuit. Also, since there is no capacitance shown as being directly connected to one terminal of the parasitic capacitance, Applicant requests that the Examiner point out why such a capacitance connected to the parasitic capacitance is "inherent".

Claim 5 recites the correction circuit as being coupled to the detection circuit for compensating for current from the input signal diverted to the parasitic capacitance due to a positive edge of the input signal. As is pointed out hereinabove, Patent '488 does not teach compensating for current change but teaches the reverse, i.e. providing positive feedback to significantly increase the difference between voltages provided to inverting and noninverting inputs of a comparator. In addition to the above, there is no teaching in any of the figures of Patent '488 that shows a capacitance employed **in addition to** the input capacitances Cin.

Claim 25 depends from claim 6 and recites that the capacitance of detection circuit has one terminal directly connected to one terminal of the parasitic capacitance which is neither taught nor remotely suggested by Patent '488 and it is submitted that claim 25 patentably distinguishes thereover for these added reasons.

The Examiner states that regarding claims 8, 9 and 20, Figure 3 of Patent '488 shows an apparatus for reducing the distortion of a signal applied to an input of a circuit at high frequency having a parasitic capacitance, comprising:

a detection circuit INV1 for detecting the change of the input signal coupled to the input; and

a correction circuit INV2 coupled to the detection circuit for compensating for current on the parasitic capacitance Cin to be added to the input signal due to a negative edge of the input signal, the Examiner stating that it should be noted that when a negative edge of the input is detected, the output of the correction circuit INV2 goes low and thus the current from the parasitic capacitance Cin is discharged to INV2 and the current from the parasitic capacitance is not added to the input signal, the Examiner further stating that it is inherent that the detection circuit INV1 includes a capacitance directly connecting to one terminal of parasitic capacitance and the parasitic capacitance Cin appears between the input and the ground. As was noted hereinabove, inverters INV1 and INV2 provide **positive** feedback and do not compensate for changes in an input voltage but, to the contrary, amplify the voltages I+ and I- applied thereto. Although the Examiner states that there is a capacitance directly connected to one terminal of the parasitic capacitance, applicant fails to see any such capacitance in any of the circuits taught

by Patent '488 and submits that no such capacitance is taught by Patent '488 and therefore requests that the Examiner point out why such a capability is "inherent".

Claim 8 positively recites a detection circuit for detecting a change in the voltage of the input signal coupled to said input and a correction circuit coupled to the detection circuit for compensating for preventing current from said parasitic capacitance to be added to the input signal due to a negative edge of the input signal. These limitations are neither taught nor even remotely suggested by Patent '488 and it is submitted that claim 8 patentably distinguishes thereover.

Claims 9 and 20 depend from claim 8 and carry all of its limitations and hence are deemed to patentably distinguish over Patent '488 for the same reasons as set forth hereinabove regarding claim 8.

Claims 1, 2, 5, 6, 12, 18, 22, 25, and 26 have been rejected under 35 U.S.C. § 102 (e) as anticipated by Diniz et al. (Patent '868). This rejection is respectfully traversed.

The Examiner states that with regard to claims 1, 2, 18, 12, 22 and 26, Figure 3 of Patent '868 shows a method for reducing distortion of a signal to an input of an input/output device having parasitic capacitance, comprising a step of:

detecting a direction of change of the input voltage (high or low) at the input;

introducing a current (64) when a positive edge of the input signal is applied to gate 48 to charge the parasitic capacitance (the Examiner notes that the parasitic

capacitance is not shown but inherently exists between the gate and source 46) to compensate the current of the input signal charging the parasitic capacitances.

The Examiner further states that it should be noted that when the input of the signal voltage is below the threshold voltage of the transistor 48, the parasitic capacitance forming between the gate-source/drain of the transistor 48 is charged and when a rising edge of the input signal is detected to be higher than the input threshold, transistor 48 is turned on and the current 64 is introduced to the parasitic capacitor to compensate for current of the input signal it charges Cin, the Examiner further stating that the parasitic capacitance Cin is across the input and ground.

The '868 Patent teaches current reference circuits which offset changes in a feed forward current such as the current 82 in Fig. 3, which alters the feed forward current by means of feedback current 84 in order to generate a sum current 85 as well as a reference voltage at an output port 86 which are insensitive to temperature, power supply and fabrication variations. There is neither any teaching or any reliance on any input capacitance or parasitic capacitance in the '868 Patent.

In the embodiment shown in Fig. 2, although there is mention of a gate oxide capacitance per unit area of transistor 44, it is stated that if the ratio of the width (W) to length (L) of transistor 44 is large, the second term in equation (1) appearing

in column 2 of line 5 can be neglected in order to provide a reliable current mirror source. There is neither teaching nor remote suggestion of any input capacitance nor of the capability of the circuitry of the Figure 2 to correct for any increases or decreases or for distortion in the current signal applied to an input of the circuit.

The objective of the invention in Patent '868 is to provide a current reference in a current mirror circuit which compensate for undesirable changes in the reference current due to supply voltage, temperature and fabrication processes.

Figure 3 of the '868 Patent provides this compensation capability through the utilization of a sensor circuit 94 which develops a feedback current 84 to compensate the feed forward current 82 generated by the Vt reference source 92 which generates a source voltage across resistor 42 that is employed to provide the feed forward current 82 by way of the current mirror structure, the gates of transistors 49 and 98 being coupled in common. Sensor 94 generates feedback current 84 responsive to the source voltage temperature variations in resistor 42, which variations cause the source voltage to change. This increases the resistance of resistor 42 causing the source voltage to increase which then causes the feed forward current 82 to **decrease**.

In contrast, the feedback current 84 will **increase** so that changes in the feed forward current are substantially offset by the changes in the feedback current. The sum current 85 which is the sum of the feed forward current 82 and the

feedback current 84 provides an output voltage at the voltage reference port 86 which is substantially constant. Thus, although the feed forward current 82 is a reference which may include an error term, the feedback current 84 includes a correction term to offset that error.

There is neither teaching nor remote suggestion of providing an input signal and compensating for an increase or decrease or a distortion in the input signal in the embodiment of Fig. 3.

The embodiment of Fig. 6 is substantially similar to that taught in Fig. 3 with modifications to stabilize a drain-to-source voltage through the use of a differential amplifier 162 coupled across the drain and gate of transistor 44 and having its output coupled to the gate of transistor 48, which differential amplifier serves to essentially reduce the drain to gate voltage of transistor 44, causing transistor 44 to substantially operate in a "virtual" diode-connected mode. A similar differential amplifier 166 is employed in the sensor circuit 94 for the same reason.

There is neither teaching nor remote suggestion of reducing distortion or changes of a signal applied to an input of a circuit having parasitic capacitance to compensate for the change in the input signal or the distortion thereof. It is therefore submitted that claims 1, 2, 18, 12, 22 and 26, whose limitations have been recited hereinabove, patentably distinguish over Patent '868.

The Examiner states that, regarding claims 5, 6 and 25 it is inherent that Figure 3 of the '868 Patent shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency and having a parasitic capacitance comprising a detection circuit 48 for detecting changes of the input voltage; a correction circuit 44, 46, 49 coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance, which, the Examiner says, although not shown, is between the gate and the source of transistor 48, due to the positive edge of the input signal, the Examiner further stating that it should be noted that when this input signal is below the threshold voltage of the circuit input the parasitic capacitance forming between the gate-source/drain of transistor 46 and the parasitic capacitor is charged and when a rising edge of the input signal is detected to be higher than the input threshold, transistor 46 is turned on and current 64 is introduced to the parasitic capacitance to compensate for current of the input signal that charges the parasitic capacitance, the Examiner stating that the parasitic capacitance is across the input gate of transistor 46 and ground.

Firstly, it should be noted that there is **no** input signal in this circuit. The '868 Patent teaches a current reference which is established by the resistor 42 which is coupled between a positive voltage V_{DD} and ground (note for example Fig. 3) with the objective of the invention of the '868 Patent being to substantially

eliminate the resistance of transistors 48 and 49 so as to have substantially no effect on the desired current reference. It is noted that the Examiner's arguments fail to indicate the location of the input of the circuit, merely making reference to the fact that the parasitic capacitance is connected across the input gate of transistor 46 and ground and further states that the correction circuit includes transistor 46. It is not understood how the transistor 46 can serve as both the input and the correction circuit. In addition to the above, there is neither teaching nor remote suggestion that either an input capacitance or a parasitic capacitance is recognized by the inventor of the '868 patent nor is there any teaching that there is any significant impact (either positive or negative) of a input capacitance or parasitic capacitance in the operation of the current reference circuit taught by the '868 Patent.

In addition, the Examiner states that the signal is applied to an input of a circuit at "high frequency". It should be noted that there is no teaching of any input signal having a high frequency since the '868 Patent teaches a current reference device having a function of maintaining the current of the current reference device constant as well as providing a voltage reference source which is constant. There is no teaching in the '868 Patent of the frequency or rate of change of reference current due to temperature, voltage or fabrication processes. It should be noted that temperature changes have the most significant effect on the reference

current/voltage and it is submitted that temperature changes do **not** occur at a "high frequency". The voltage reference port is port 86 shown in Fig. 83 and the current reference is the current 91 of the system 90 which is described as providing either a constant reference current or reference resistance. For these reasons it is submitted that claims 5, 6 and 25 which recite the limitations set forth above in response to the arguments regarding the '488 Patent, patentably distinguish over the '868 Patent.

In view of the foregoing comments, it is submitted that claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23 and 25-27 patentably distinguish over the art of record and reconsideration and allowance of these claims are earnestly solicited.

Favorable action is awaited.

Respectfully submitted,

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